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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,452	09/26/2001	Andrew Marshall	TI-28975	5345

23494 7590 06/03/2004

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EXAMINER	
TANG, MINH NHUT	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/965,452	MARSHALL ET AL.
	Examiner	Art Unit
	Minh N. Tang	2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on March 08, 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4, 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-2, 4, and 9-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claims 1, the limitation "said probe pad configured also as an output pad from which response of the selected test structure to the input voltage may be taken" is not supported by the original specification.

In claim 9, the limitation "[a]nd from said probe pad response of the selected test structure to the input voltage may be taken" is not supported by the original specification.

In claim 12, the limitation "taking measurement of the electrical characteristics of the selected one of said multiple test structures at the probe pad" is not supported by the original specification.

It is noted that the original specification does not disclose a probe pad that is used both as an input pad for applying an input voltage and as an output pad for measuring the response of the selected test structure. For examination purposes, those

limitations above are not considered until Applicants clarify the supporting of the claims' limitations.

Claims 2, 4, and 10-11 are rejected since they depend on rejected base claims.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-2, 4, and 9-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the limitation "the selected test structure" (lines 6-7) has not been recited previously; therefore this term is indefinite. Furthermore, a limitation followed by linking terms (e.g., preferably, may be, for instance, especially) is considered indefinite since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired.

In claim 9, a limitation followed by linking terms (e.g., preferably, may be, for instance, especially) is considered indefinite since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired.

Claims 2, 4, and 10-11 are rejected since they depend on rejected base claims.

Claim Objections

5. Claim 12 is objected to because of the following informalities: in claim 12, line 2, "multiple test structure" should be -- multiple test structures --. Appropriate correction is required.

Claim R j ctions - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2, 4, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freed (U.S.P. 3,781,683) in view of Hubacher (U.S.P. 3,849,872).

As to claim 1, Freed discloses, in Fig. 2, a wafer having a probe pad (30-38), comprising: multiple test structures (i.e., odd and even testing circuits repeatedly formed in the kerf, hereafter testing circuits) selectably multiplexed (i.e., transmitting signals through testing circuits) to said probe pad (30-38). Freed does not explicitly disclose applying an input voltage to probe pad (30-38). Hubacher discloses, in Figs. 1 and 2, a test system for selectively activating a chip (35) comprising a transistor (25) formed in the wafer kerf having a base (29), a collector (28) and an emitter (30), a voltage signal

(+V) being applied to the collector (28) and a simultaneous signal being applied to the base (29) of the transistor (25), respectively, in order to select a particular transistor for producing a higher voltage output on the emitter (30). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the apparatus of Freed by providing an appropriate input voltage to the collector and the base of the transistor (i.e., pad 31, pad 37 connected to collector and base of transistor T2 in Freed reference) as taught by Hubacher so that a corresponding voltage would produce at the emitter of the transistor.

As to claims 2 and 10, Freed discloses in Fig. 2, said probe pad (30-38) is located in a scribeline (vertical kerf 11), and occupies more than half (see, for example pads 36, 38) the width of said scribeline (11).

As to claims 4 and 11, Freed in view of Hubacher disclose said multiple test structures (testing circuits) are selectively multiplexed to said probe pad (30-38) in dependence on sequence of voltages (i.e., voltage applied to the collector and the base of the transistor T2) applied to said probe pad (30-38).

As to claims 9 and 12, Freed discloses, in Figs. 2 and 3, a scribeline test circuit, comprising: a test selector circuit (T2) located in a single scribeline portion (kerf 11) between two adjacent die locations (i.e., between dice 10); multiple test structures (i.e., odd and even testing circuits repeatedly formed in the kerf, hereafter testing circuits), also located in said single scribeline portion (11); and at least one probe pad (30-38), also located in said single scribeline portion (11) communicable to the multiple test structures (testing circuits); wherein said test selector circuit (T2) makes an electrical

connection from said probe pad (30-38) only to a selected one (i.e., odd testing circuit) of said test structures (testing circuits). Freed does not explicitly disclose applying an input voltage at said probe pad (30-38). Hubacher discloses, in Figs. 1 and 2, a test system for selectively activating a chip (35) comprising a transistor (25) formed in the wafer kerf having a base (29), a collector (28) and an emitter (30), a voltage signal (+V) being applied to the collector (28) and a simultaneous signal being applied to the base (29) of the transistor (25), respectively, in order to select a particular transistor for producing a higher voltage output on the emitter (30). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the apparatus of Freed by providing an appropriate voltage to the collector and the base of the transistor (i.e., pad 31, pad 37 connected to collector and base of transistor T2 in Freed reference) as taught by Hubacher so that a corresponding voltage would produce at the emitter of the transistor.

Response to Arguments

4. Applicant's arguments with respect to claims 1-2, 4, and 9-12 have been considered but are moot in view of the new ground(s) of rejection.

In response to Applicant's argument, throughout the Remarks, that both the Freed reference and the Hubacher reference do not disclose using a probe pad both as input for selecting the circuit under test and as output pad to measure the response of the circuit to the input voltage, it is noted that the features upon which applicant relies are not supported by the original specification.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mrs. Cuneo, Kamand can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Minh Tang
May 19, 2004

David A. Zarneke
Primary Exam
5/28/04